

Fig. 1

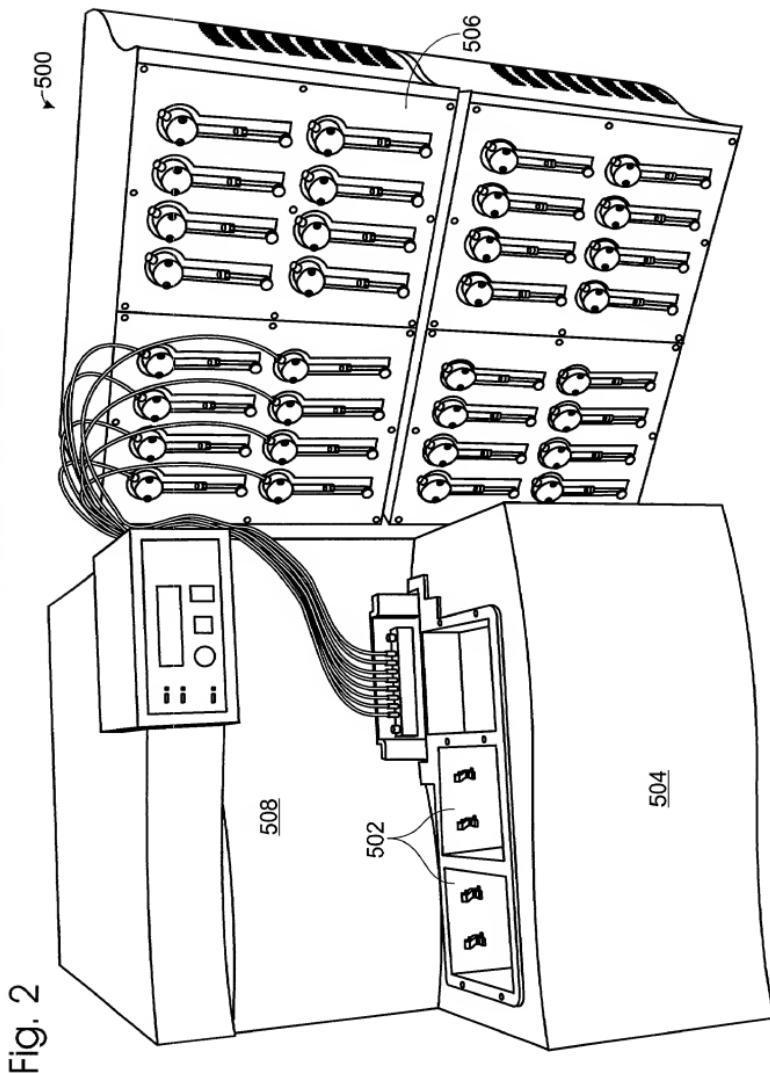


Fig. 3

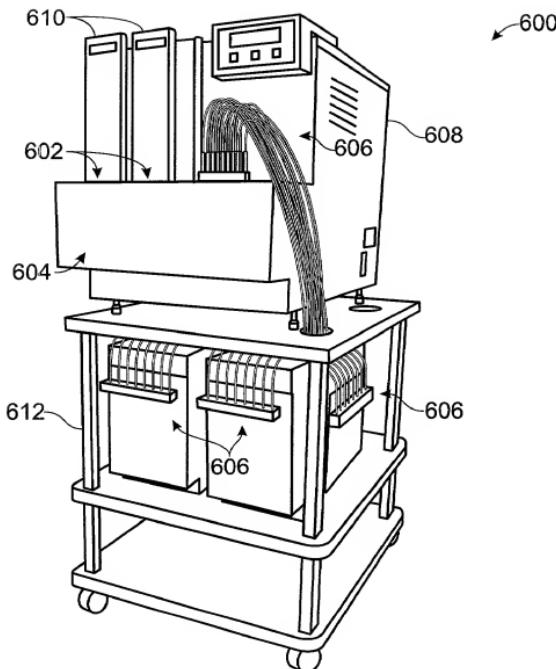
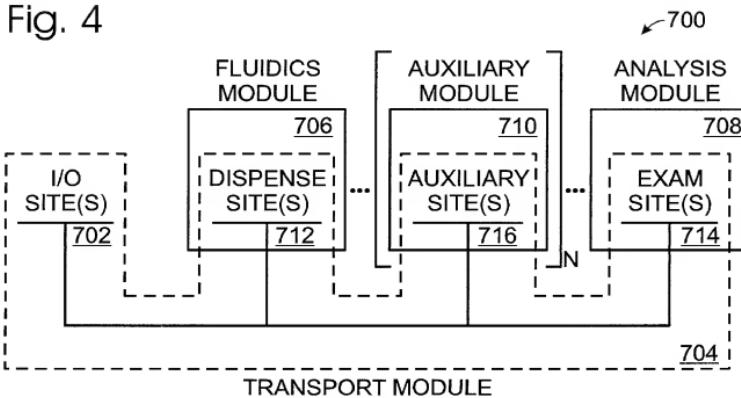
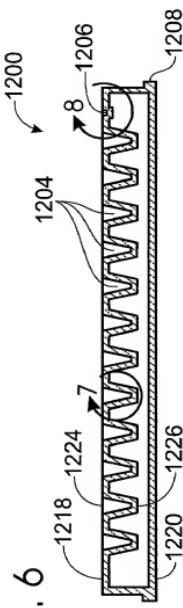
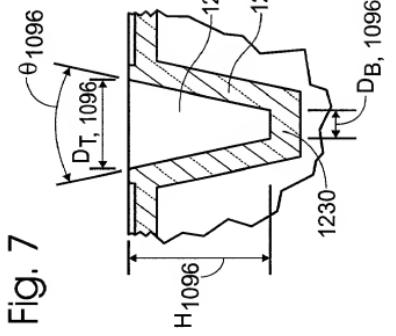
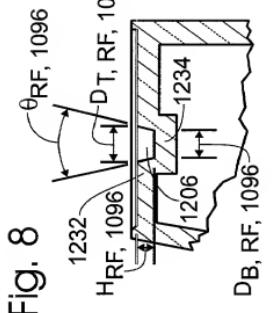
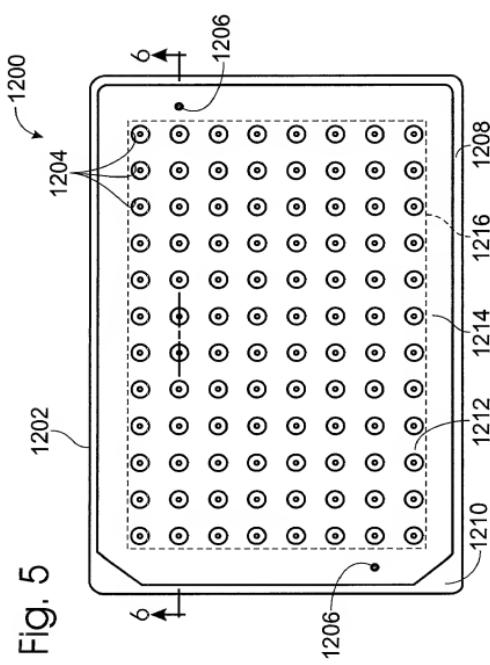


Fig. 4





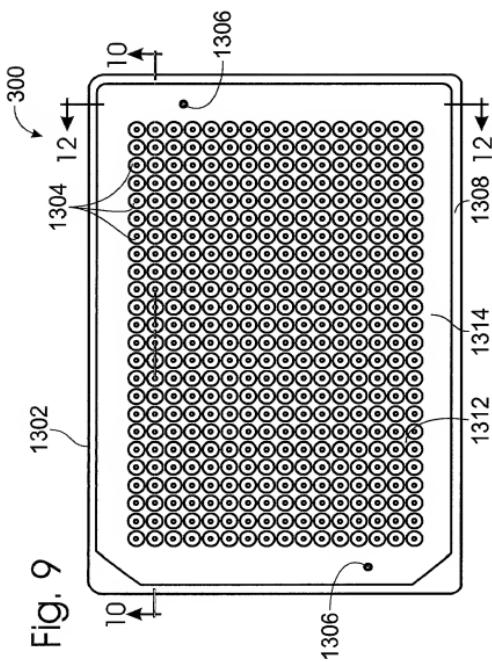


Fig. 12

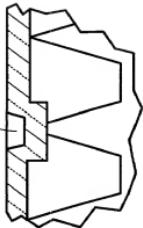
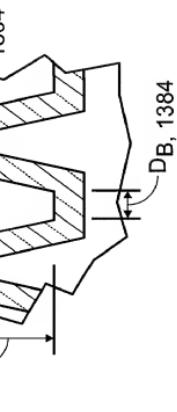
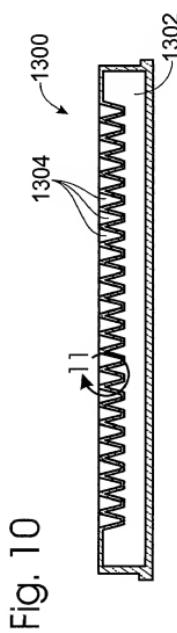
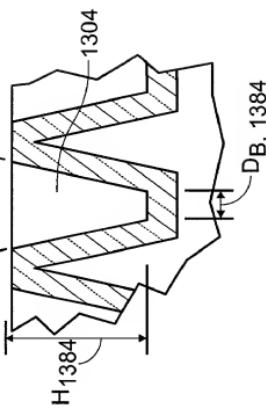


Fig. 11



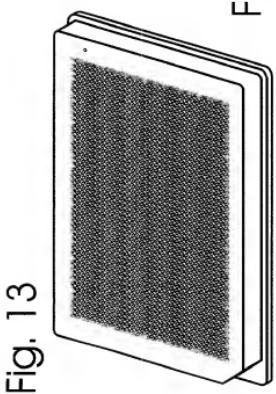


Fig. 13

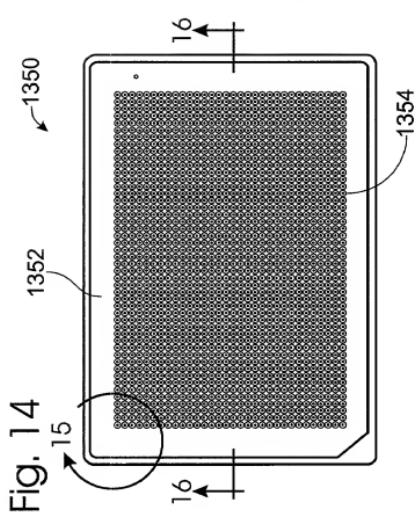


Fig. 14

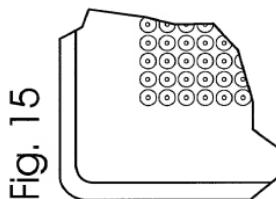


Fig. 15

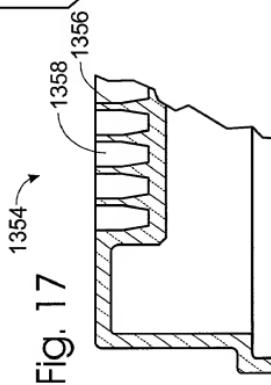


Fig. 17

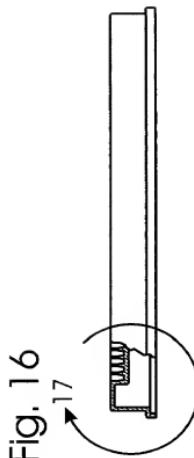


Fig. 16

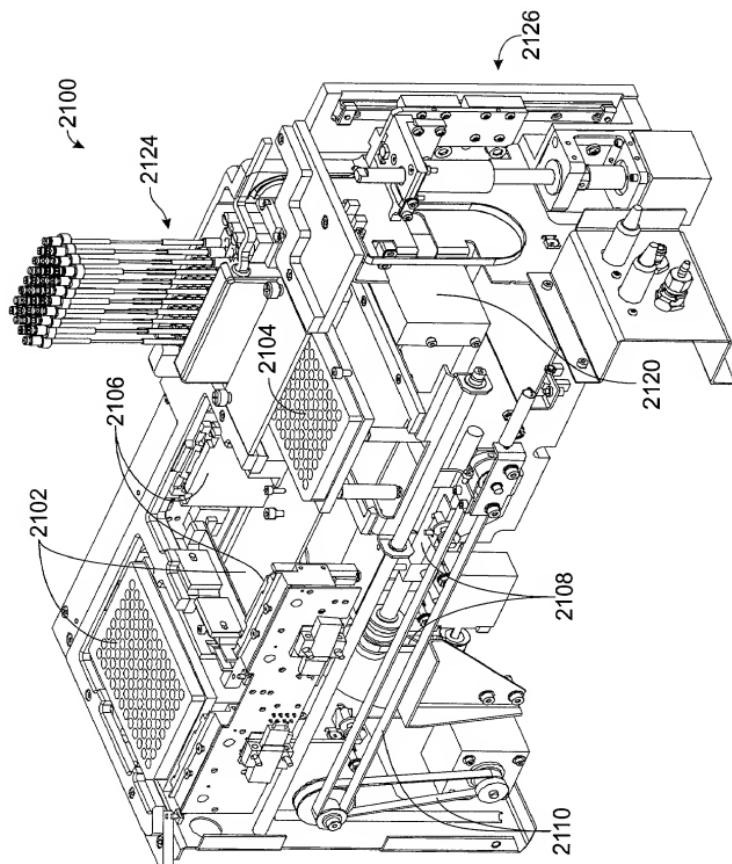


Fig. 18

Fig. 19

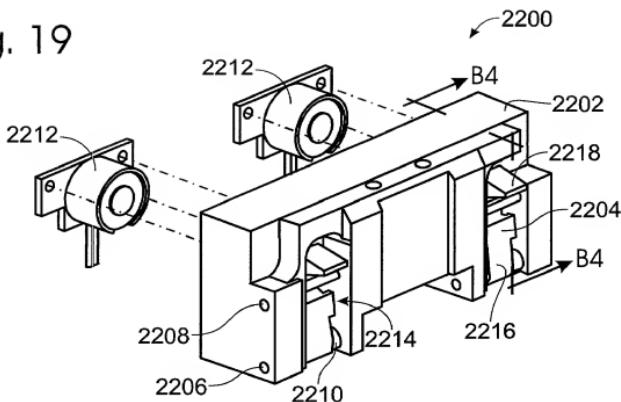


Fig. 20

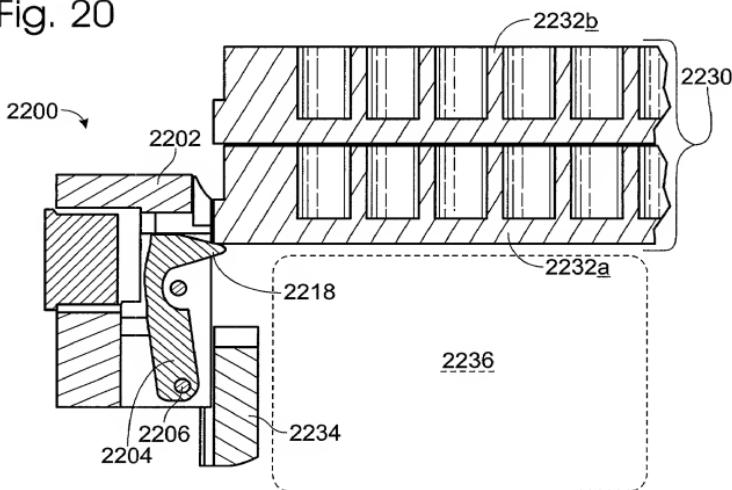


Fig. 21 (INPUT CYCLE)

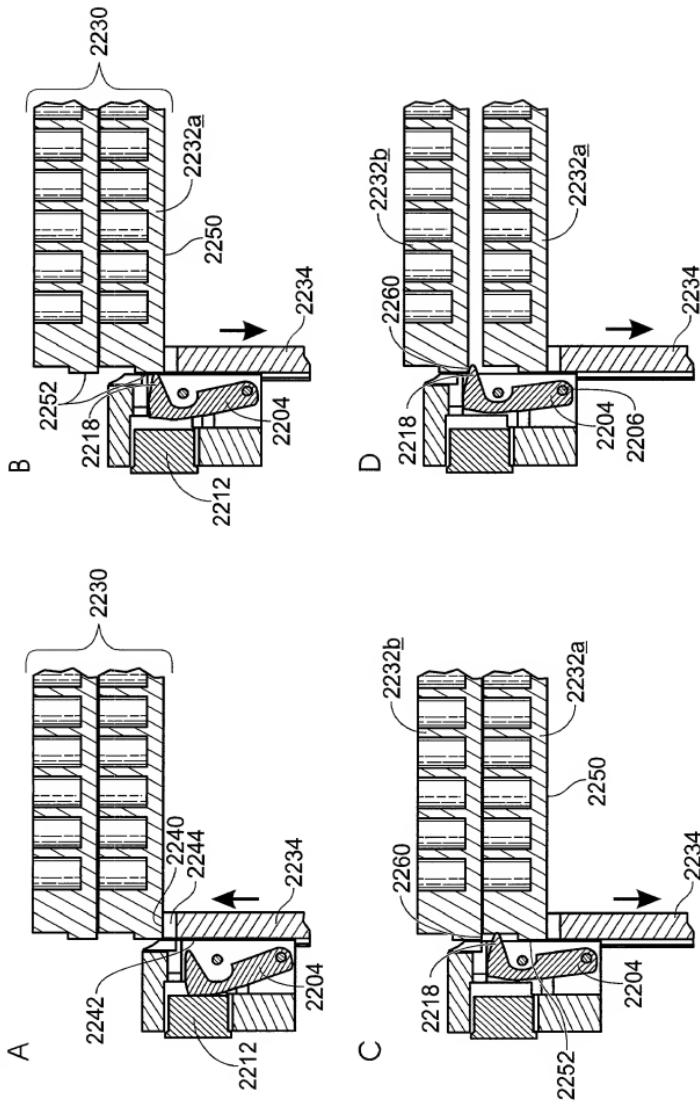


Fig. 22 (OUTPUT CYCLE)

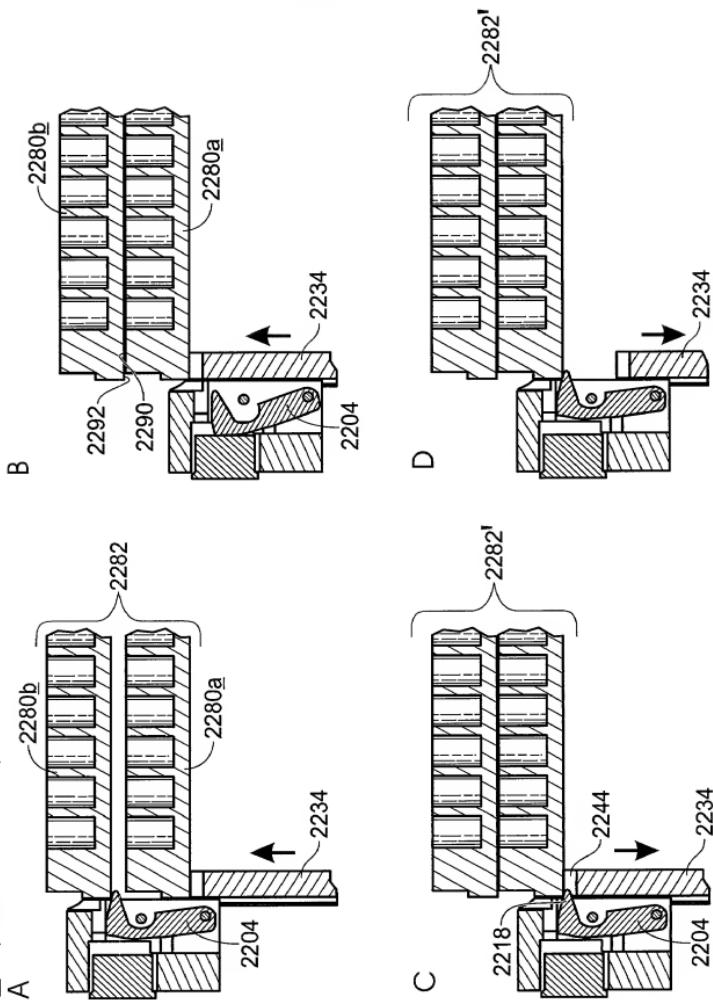
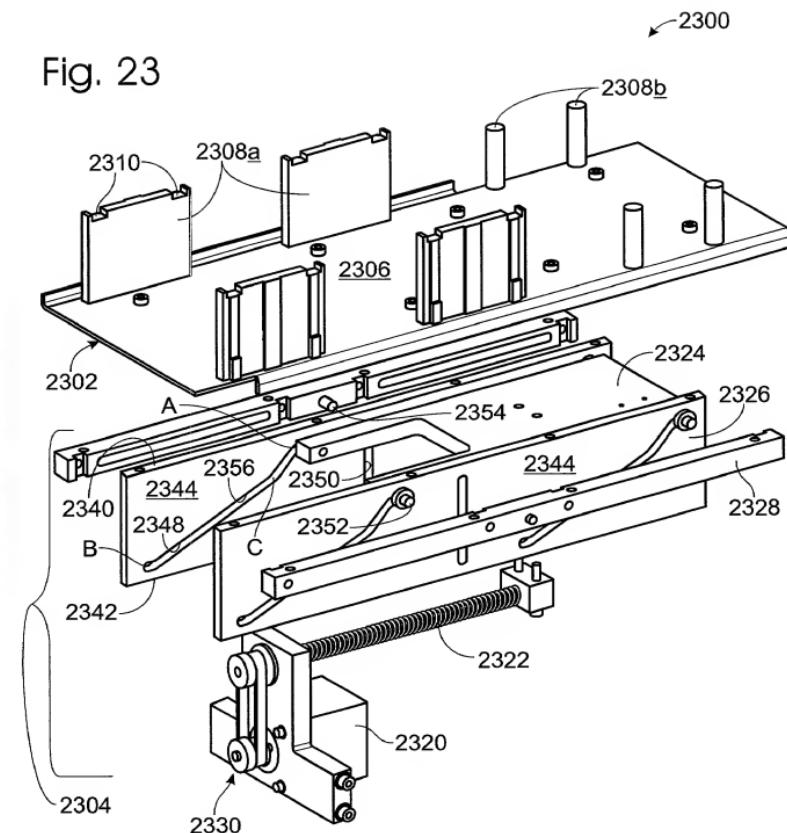


Fig. 23



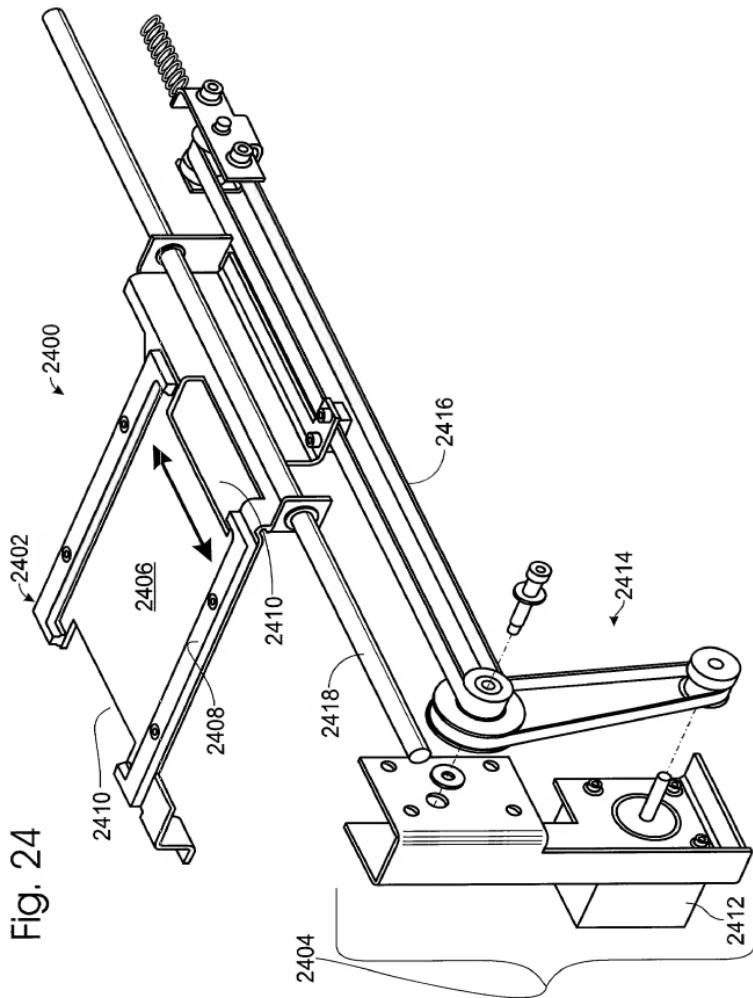


Fig. 24

Fig. 25

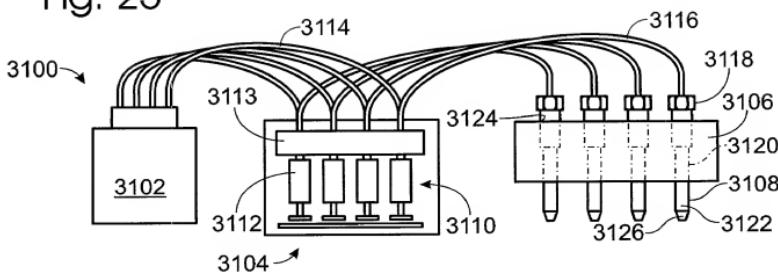


Fig. 26

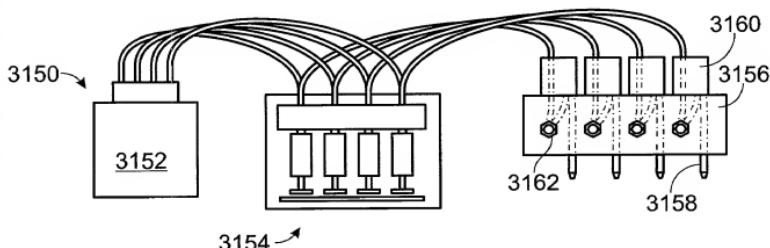


Fig. 27

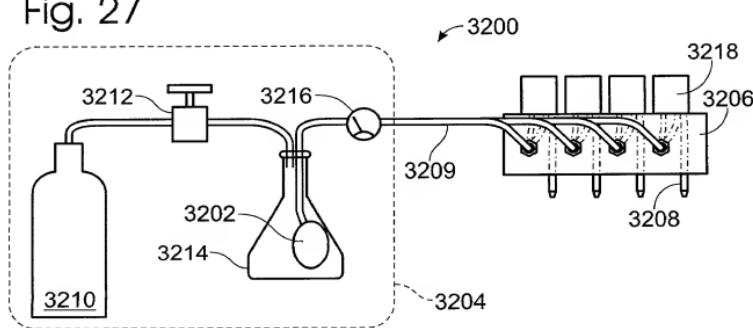


Fig. 28

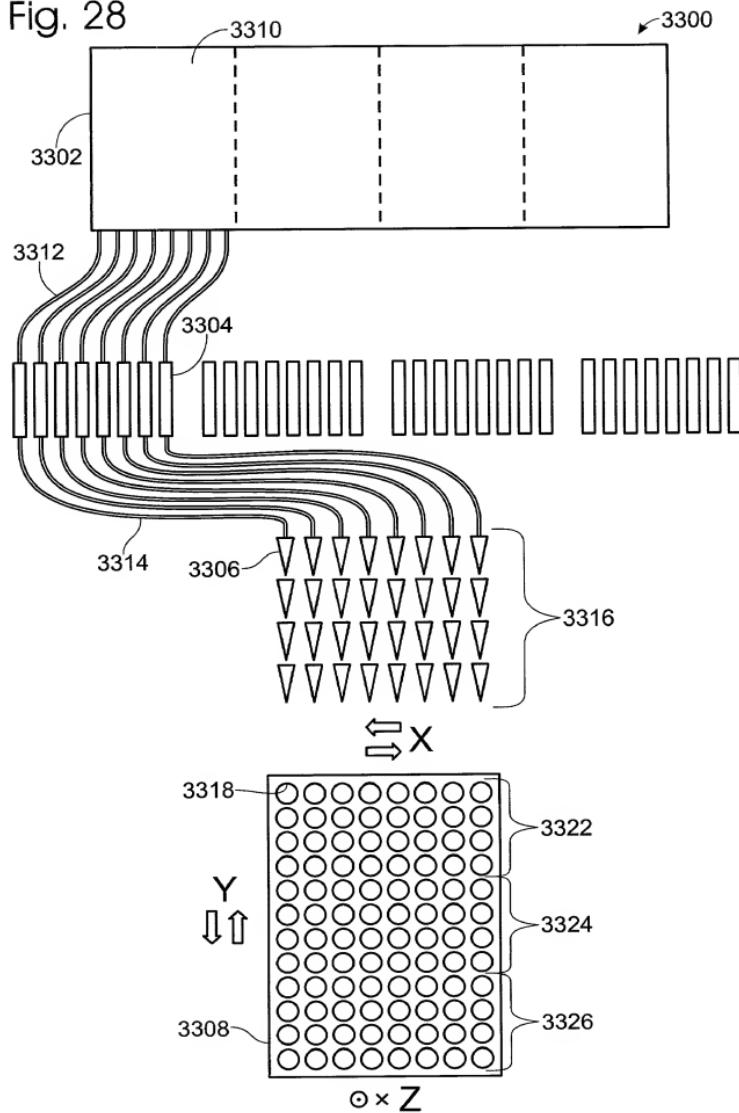


Fig. 29

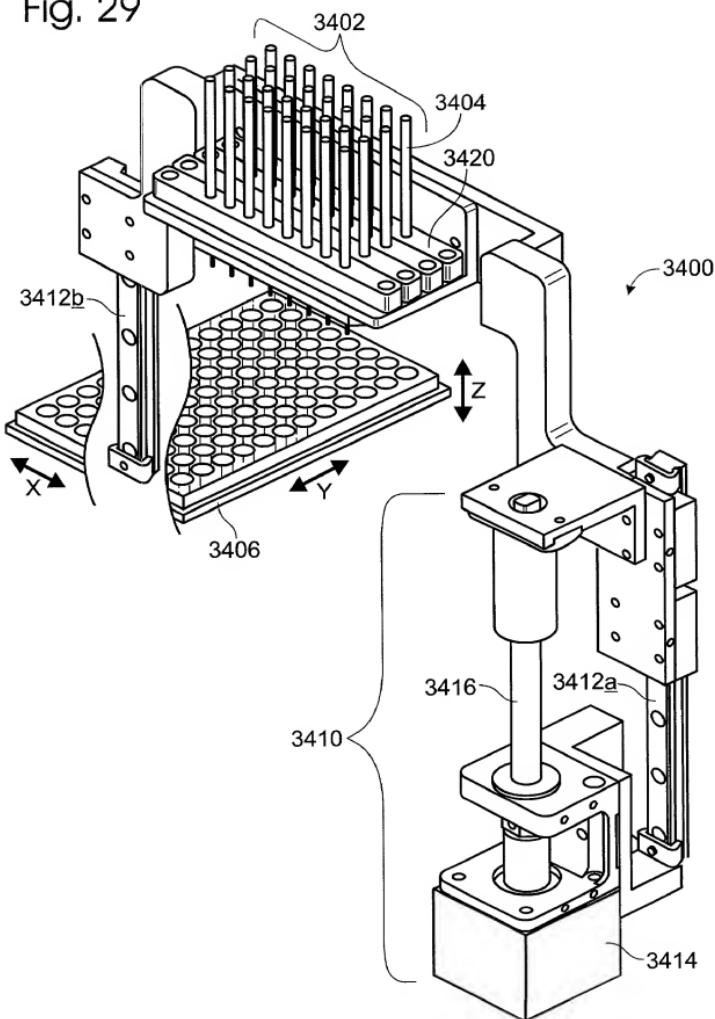


Fig. 30

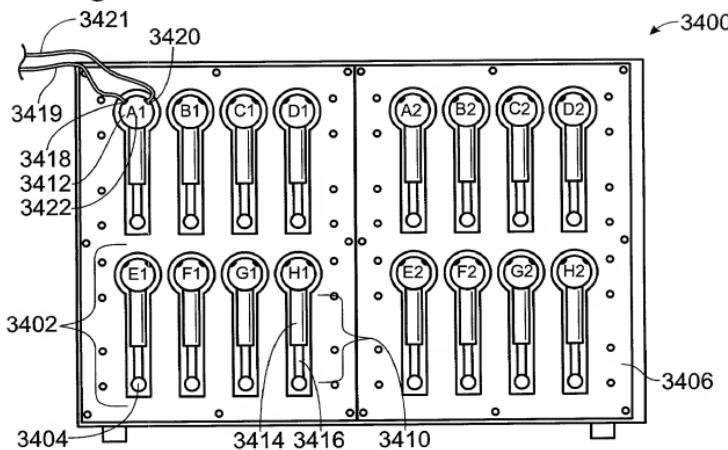


Fig. 31

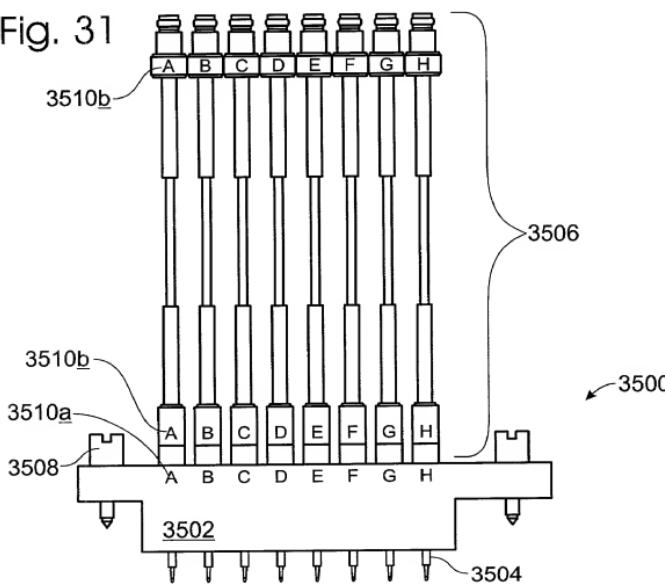


Fig. 32

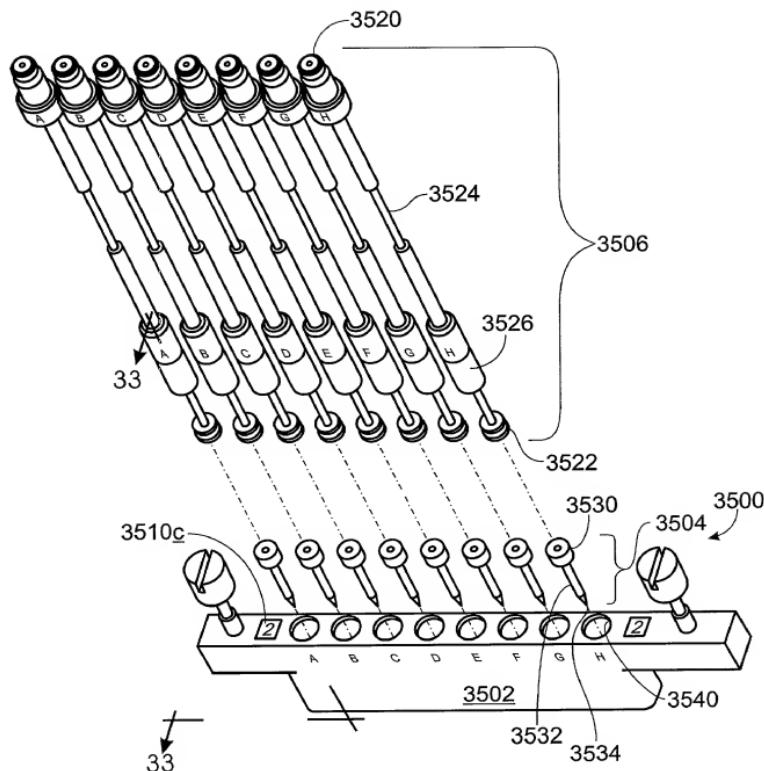


Fig. 33

